
SECTION IX

FREQUENCY DOMAIN FUNCTIONS:

D/A CONVERSION AND DIRECT DIGITAL SYNTHESIS

FREQUENCY DOMAIN FUNCTIONS: D/A CONVERSION AND DIRECT DIGITAL SYNTHESIS

APPLICATIONS FOR HIGH SPEED DACs

**DYNAMIC PERFORMANCE CONSIDERATIONS
AND SPECIFICATIONS FOR DACs**

**Settling Time, Update Rate, Glitch Impulse,
Harmonic Distortion, Phase Noise**

SIN X/X ROLLOFF EFFECT

HIGH SPEED DAC IMPLEMENTATIONS

DESIGNING FOR MINIMUM GLITCH IMPULSE

GLITCH REDUCTION USING SEGMENTATION

DEGLITCHING USING SHA_s

DIRECT DIGITAL SYNTHESIS TECHNIQUES

FREQUENCY SYNTHESIS FIGURES OF MERIT

DIRECT DIGITAL SYNTHESIS APPLICATIONS

APPLICATIONS FOR DACS

High-speed D/A converters (DACs) have wide applications in instrumentation, waveform reconstruction and generation, and direct digital synthesis (DDS). A new class of function generators called Arbitrary Waveform Generators allow a wide variety of complex waveforms to be programmed into a memory and then read out through a DAC.

Graphics display systems also utilize high-speed DACs to direct and/or modulate the scanning electron beam across the CRT screen. Vector scan display systems and raster scan display systems are the two

most popular video displays in use today. A special type of high-speed DAC, sometimes referred to as a "VIDEODAC", contains functions which allow ease of use in raster scan display systems. Some newer videodacs contain color palette memories and are often referred to as "RAMDACs".

High-speed DACs are essential building blocks for successive approximation and digitally corrected subranging A/D converters. This application has been discussed previously in the section on A/D Conversion.

DYNAMIC PERFORMANCE CONSIDERATIONS AND SPECIFICATIONS FOR DACS

Settling time of a DAC is traditionally defined as the time from the digital input transition (usually measured from the 50% point) until the DAC output settles to within a certain error band (usually $\pm 1/2$ LSB) which is centered around the final value. As shown in Figure 9.2, a portion of the settling time may be due to a fixed propagation delay through the switches. If the DAC has a set of input latches or registers, the settling time is measured from the 50% point of the latch strobe or register clock. Fullscale DAC settling time is measured for a digital input transition from 000...0 to 111...1. Midscale settling time is measured for a digital transition from 011...1 to 100...0 or 100.0 to 011...1.

DAC *update rate* must be considered in conjunction with settling time and propagation delay in order to be a meaningful spec. Typically, the maximum update rate is the reciprocal of the difference between the settling time and the propagation

delay. Updating the DAC faster will cause errors since the output is not given enough time to settle to within $\pm 1/2$ LSB. This situation may be acceptable in some applications - especially where the maximum digital input change between updates is limited to a few LSBs.

HIGH SPEED DAC APPLICATIONS

- **Instrumentation**

- Waveform Reconstruction**

- Arbitrary Waveform Generators**

- **Direct Digital Synthesis (DDS)**

- **Graphics Display Systems**

- Vector Scan**

- Raster Scan - Videodacs, Ramdacs**

- **A/D Converters**

- Successive Approximation**

- Digitally Corrected Subranging (DCS)**

Figure 9.1

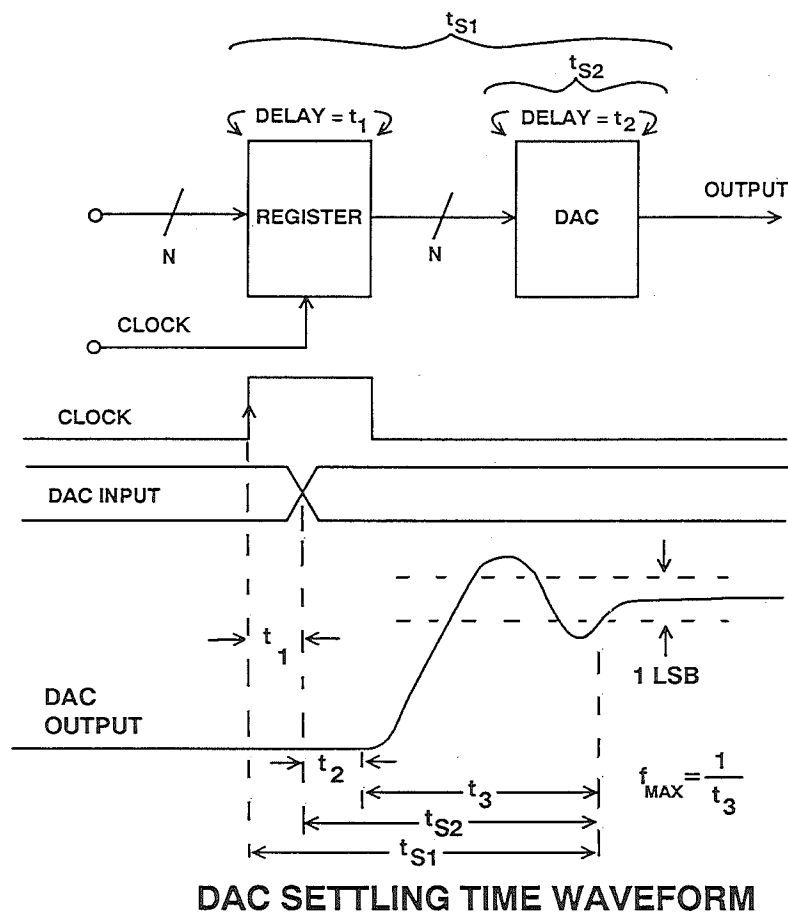
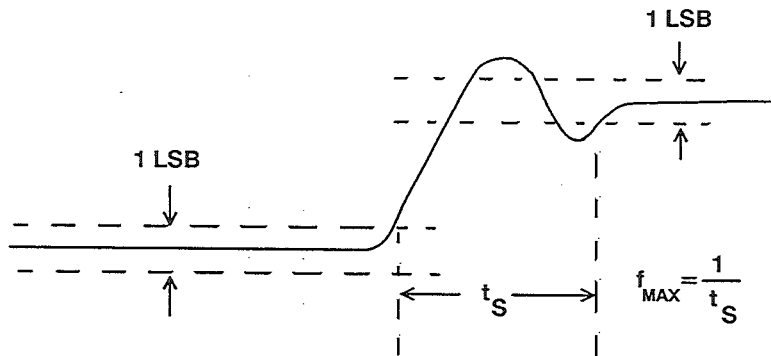


Figure 9.2

It is entirely correct to define DAC settling time with respect to the output alone as shown in Figure 9.3. Settling time is measured from the time the output leaves a $\pm 1/2$ LSB error band centered around the initial value until the time the output remains within a $\pm 1/2$ LSB error band centered around the final value. The maximum DAC update rate allowable for $\pm 1/2$ LSB settling time then becomes:

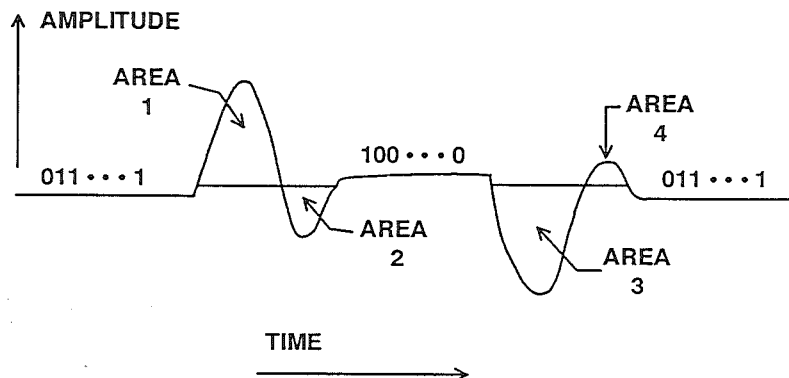
$$f_{\text{MAX}} = \frac{1}{t_s}$$

This technique effectively removes the propagation delay due to the input registers and the DAC switches from the measurement. Window comparators are useful in performing this measurement.



SETTLING TIME REFINED WITH RESPECT TO DAC OUTPUT

Figure 9.3



GLITCH IMPULSE AREAS: AREA 1
AREA 2
AREA 3
AREA 4

NET GLITCH IMPULSE AREAS: | AREA 1 - AREA 2 |
| AREA 3 - AREA 4 |

GLITCH IMPULSE WAVEFORMS

Figure 9.4

Glitch impulse area is best understood by examining the waveform shown in Figure 9.4. DAC glitches occur because of digital input logic skew and unequal propagation delays through the DAC switches. The glitches are usually the largest at the midscale transition because all bits in the DAC are changing at this point. The glitch produced by the 011...1 to 100...0 transition is usually different from that produced by the 100...0 to 011...1 transition, so each must be analyzed. *Glitch impulse area* is simply the area of a particular glitch and is usually measured in the units of pV-sec, therefore the fullscale output voltage of the DAC must be known in order to make meaningful comparisons between DACs. The term "glitch energy" is incorrect since the unit pV-sec is *not* a measure of energy.

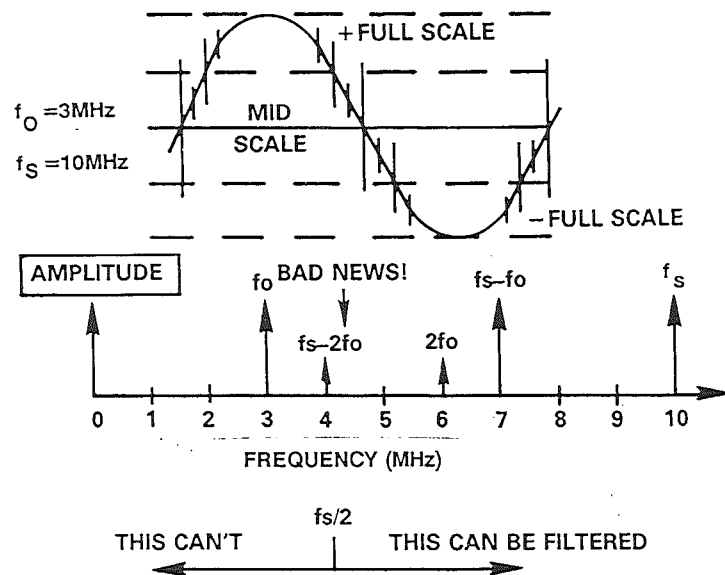
Glitches may also be caused by charge coupling by stray capacitance between the digital and analog regions of the DAC. These glitches are unaffected by reference amplitude so may be measured, independent of skew-related glitches, by measurements made in the absence of a reference voltage.

From Figure 9.4 it is clear that there are six possible glitch impulse areas to deal with. There are two glitch impulses associated with each transition. Their respective areas are designed 1, 2, 3 and 4. In addition, it is also useful to consider the *net glitch impulse area* associated with each of the two transitions. There are, respectively, $\text{AREA 1} - \text{AREA 2}$, and $\text{AREA 3} - \text{AREA 4}$. When examining the glitch impulse area specification on a DAC data sheet, it is therefore clear that there is much room for confusion unless a considerable amount of clarification is provided by the manufacturer.

Glitch impulse area remains constant regardless of filtering. Fast settling time specifications do not always imply low glitch impulse areas. The desirable situation is for the DAC to have a net glitch impulse area of zero for each of the two transitions, i.e., $\text{AREA 1} - \text{AREA 2} = \text{AREA 3} - \text{AREA 4} = 0$. In the ideal case, of course, $\text{AREA 1} = \text{AREA 2} = \text{AREA 3} = \text{AREA 4} = 0$.

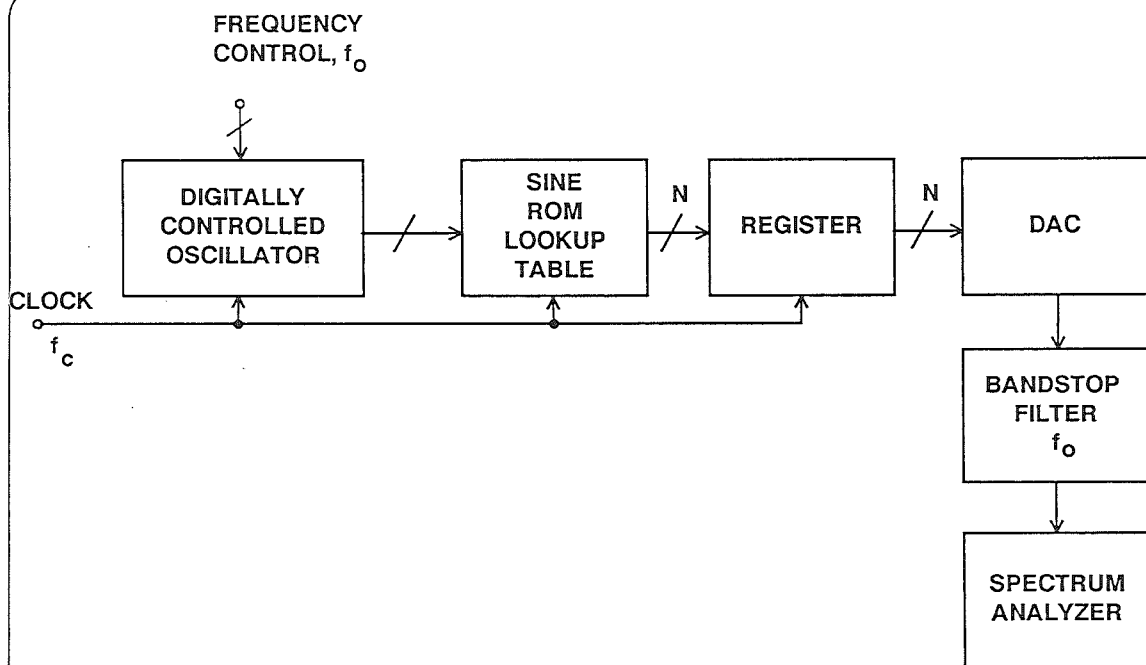
Because the net glitch impulse area is code dependent, it will produce harmonics when the DAC is reconstructing a sinewave. A net midscale glitch occurs twice during a single cycle of the reconstructed sinewave (at each zero crossing) and, therefore, will produce a second harmonic of the sinewave as shown in Figure 9.5. As shown in Figure 9.5, higher order harmonics of the fundamental sinewave which alias back into the Nyquist bandwidth are not filterable. It is difficult to predict the harmonic distortion caused by a specified net glitch impulse area, therefore, both specifications are required to adequately evaluate the dynamic performance of a high-speed DAC.

Distortion present at the output of a DAC reconstructing a sinewave from a ROM can be measured directly using an analog spectrum analyzer as shown in Figure 9.6. It is often useful to insert a bandstop filter between the DAC and the analyzer input in order to prevent erroneous readings due to overdriving the analyzer's front end amplifier. As with A/D converters, the harmonic distortion levels in a DAC are not necessarily related to the DAC resolution. It is entirely possible for a low-glitch 8-bit ECL DAC such as the AD9768 to have lower harmonic distortion levels than a 12-bit TTL DAC such as the AD-568.



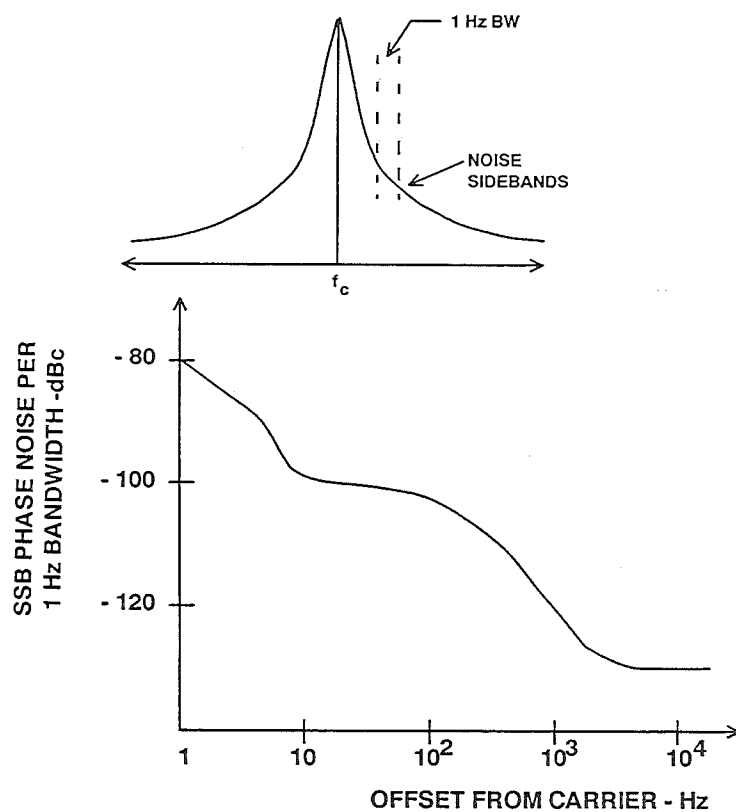
EFFECTS OF DAC GLITCHES

Figure 9.5



MEASURING DAC HARMONIC DISTORTION

Figure 9.6



SINGLE-SIDED PHASE NOISE SPECTRAL DENSITY

Figure 9.7

Various techniques for reducing the glitch impulse area of a DAC (and thereby reducing harmonic distortion) will be discussed later in this section.

Phase noise of a reconstruction DAC is measured and specified in a manner similar to that of a high quality frequency synthesizer. The noise specification that is most widely used in the signal generator industry is the single-sided phase noise spectral density as shown in Figure 9.7. The spectral density is a plot of the noise power per Hertz bandwidth as a function of frequency offset from the carrier frequency.

Direct measurement of this spectral density function with a spectrum analyzer may not be possible, and the signal may have to be demodulated to baseband in order to obtain the measurement with low-frequency instruments.

As high-speed, high-resolution reconstruction DACs begin to proliferate in the field of arbitrary waveform generation and direct digital synthesis, dynamic performance specifications such as harmonic distortion and phase noise will begin to become commonplace on DAC data sheets.

SINX/X FREQUENCY ROLLOFF EFFECT

The output of a reconstruction DAC can be visualized as a series of rectangular pulses whose width is equal to the reciprocal of the update rate (see Figure 9.8). The frequency response is given by the equation:

$$A = \frac{\sin\left(\frac{\pi f_o}{f_c}\right)}{\frac{\pi f_o}{f_c}}$$

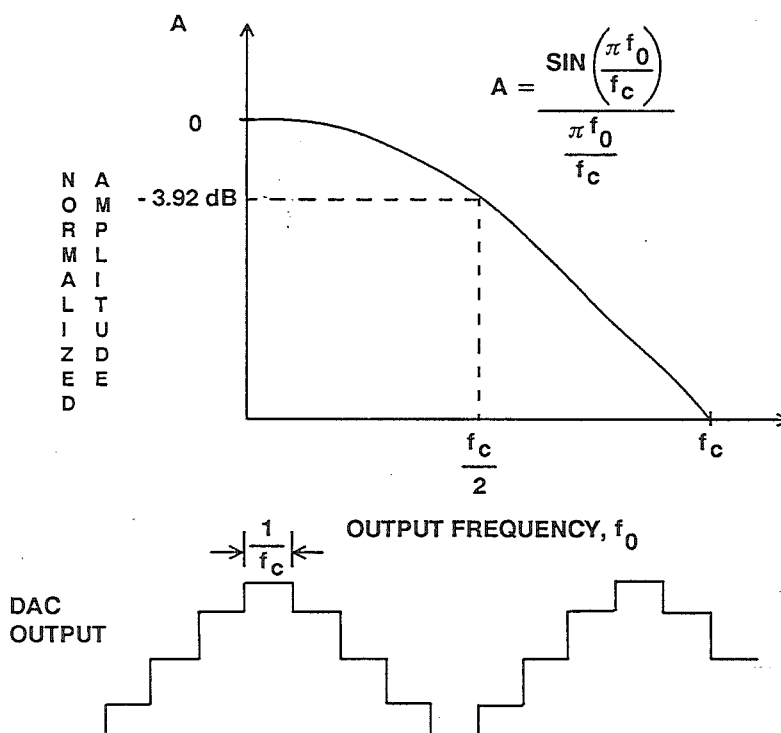
where

A = normalized output amplitude

f_c = DAC update frequency

f_o = reconstructed output frequency

Note that the reconstructed signal is down 3.92dB at the Nyquist limit with respect to the low frequency value. An "inverse" SINX/X filter is sometimes placed after the DAC to correct for this effect.



SIN X/X ROLLOFF

Figure 9.8

HIGH SPEED DAC IMPLEMENTATIONS

Most DACs consist of two basic elements: a set of current switches and a method for binary current division. Figure 9.9 shows two methods for constructing a DAC. In the first method, the current switches carry equal currents and the binary scaling is done with a R-2R resistor network. The second method utilizes binarily weighted current sources whose switched outputs are summed together.

Some high-speed DACs use a combination of the two methods: binarily weighted current switches for the MSBs followed by R-2R current division for the LSBs.

Differential pairs are often utilized for the actual current switches. Figure 9.10 shows a typical PNP current switch for a TTL DAC (AD-568) and an NPN switch for an ECL DAC (AD9768).

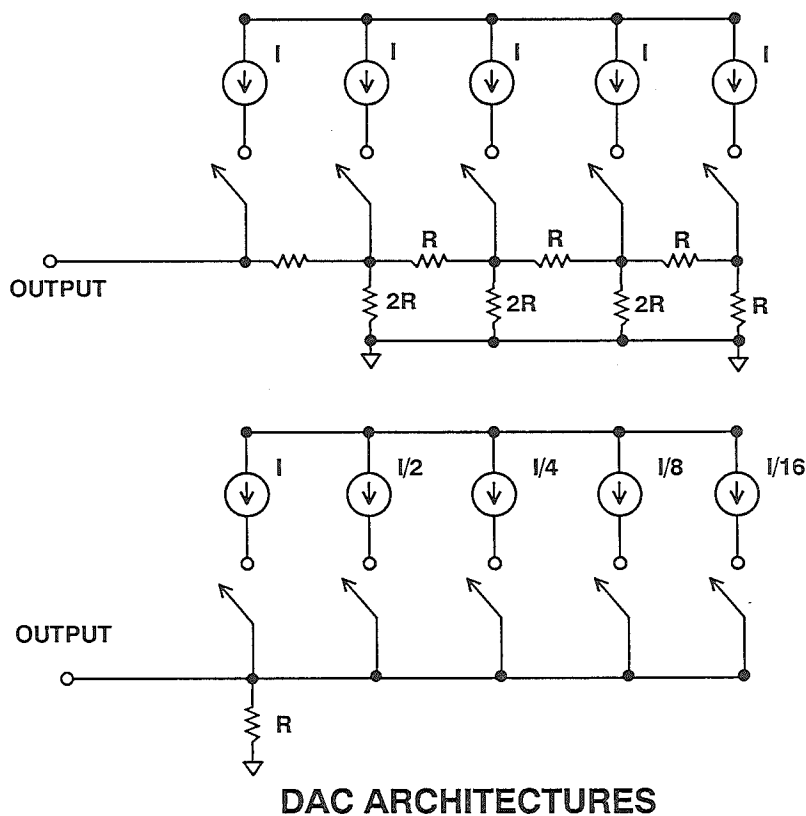
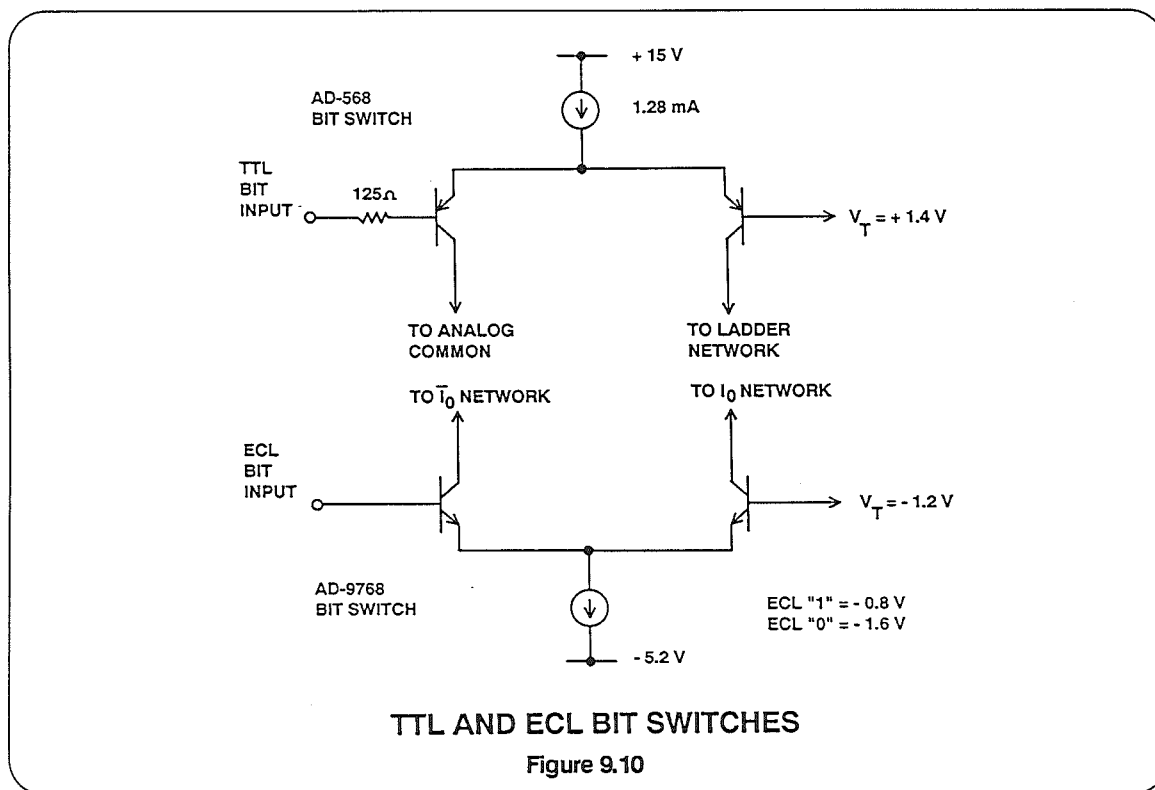


Figure 9.9



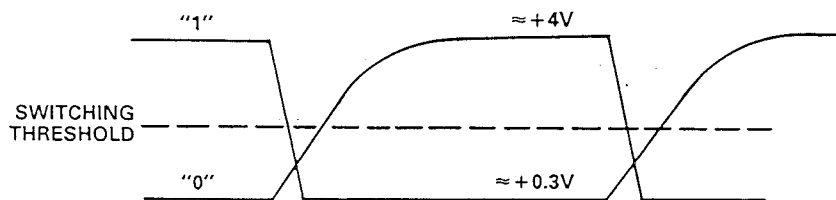
DESIGNING FOR MINIMUM GLITCH IMPULSE

Most low glitch high-speed DACs are designed around differential NPN switches which are driven by ECL logic levels. ECL logic swings are symmetrical and have an amplitude which is more than sufficient to switch a differential pair. TTL logic swings on the other hand are not symmetrical and have propagation delays which depend upon the direction of the logic transition as shown in Figure 9.11. HCMOS and fast logic swings are more symmetrical than standard bipolar TTL and provide a better choice for driving high-speed TTL DACs such as the AD-568. The effect of drive logic on the dynamic performance of the 12-bit AD-568 DAC is shown in Figure 9.12.

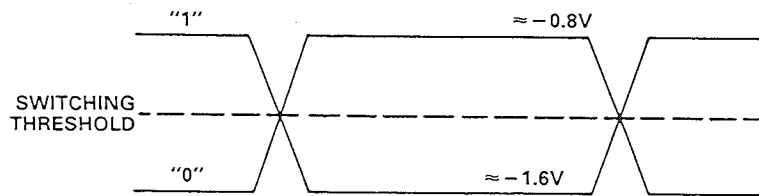
Deskewing is a technique which is often used to reduce the glitch impulse. This

amounts to equalizing the delay of the first two or three most significant bits by the use of an external RC network as shown in Figure 9.13. The resistors and capacitors are adjusted until both the 011...1 to 100...0 and the 100...0 to 011...1 glitch have been minimized. Some high-speed DACs such as the AD-568 have the capability of externally "tweaking" the switching logic voltage threshold and thereby reducing the data skew further. The effects of this threshold adjustment for the AD-568 are shown in Figure 9.14.

ECL DACs such as the 8-bit AD9768 can be effectively deskewed using capacitors as shown in Figure 9.15. Using this technique, it is possible to reduce the glitch impulse to less than 100pV-sec.



TTL LOGIC SWITCHING



ECL LOGIC SWITCHING

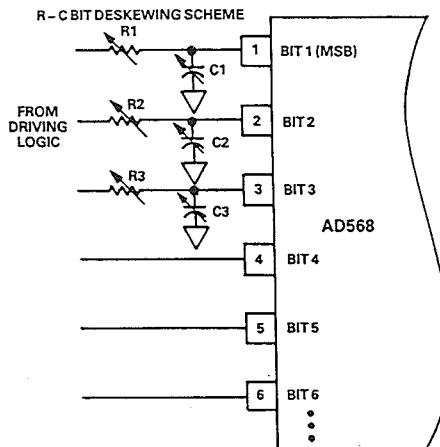
TTL AND ECL LOGIC TRANSITIONS

Figure 9.11

AD-568 DAC PERFORMANCE VS. DRIVE LOGIC

Logic Family	10-90% DAC Rise Time	DAC Settling Time			Glitch Impulse	Maximum Glitch Excursion
		1%	0.1%	0.025%		
TTL	11ns	18ns	34ns	50ns	2.5nV-s	240mV
LSTTL	11ns	28ns	46ns	80ns	950pV-s	160mV
STTL	9.5ns	16ns	33ns	50ns	850pV-s	150mV
HCMOS	11ns	24ns	38ns	50ns	350pV-s	115mV
FAST*	12ns	16ns	36ns	42ns	1.0nV-s	250mV

Figure 9.12



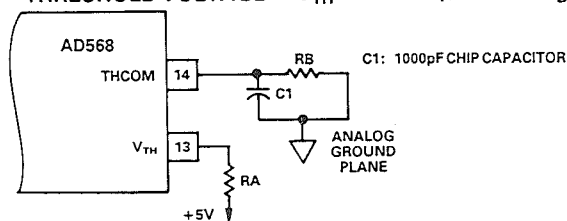
Logic Family	Gate	Uncompensated Glitch	Compensation Used	Compensated Glitch
HCMOS	74157	350pV-s	C2 = 5pF	250pV-s
STTL	74158	850pV-s	R1 = 50Ω, C1 = 7pF	600pV-s

R and C Values = 0 Unless Otherwise Noted

EFFECTS OF DESKEWING ON AD-568 GLITCH

Figure 9.13

SELECTING RA AND RB:
 $RA + RB = 5V/3.6mA$
THRESHOLD VOLTAGE = $V_{TH} = 1.4V + (3.6mA \times R_B)$



POSITIVE THRESHOLD VOLTAGE SHIFT

THRESHOLD SHIFT FOR GLITCH IMPROVEMENT¹

Logic Family	Gate	Uncompensated Glitch	Modified Threshold ²	Resulting Glitch
HCMOS	74HC158	350pV-s	1.7V	150pV-s
STTL	74S158	850pV-s	1.0V	200pV-s
FAST	74F158	1000pV-s	1.3V	480pV-s

NOTES:

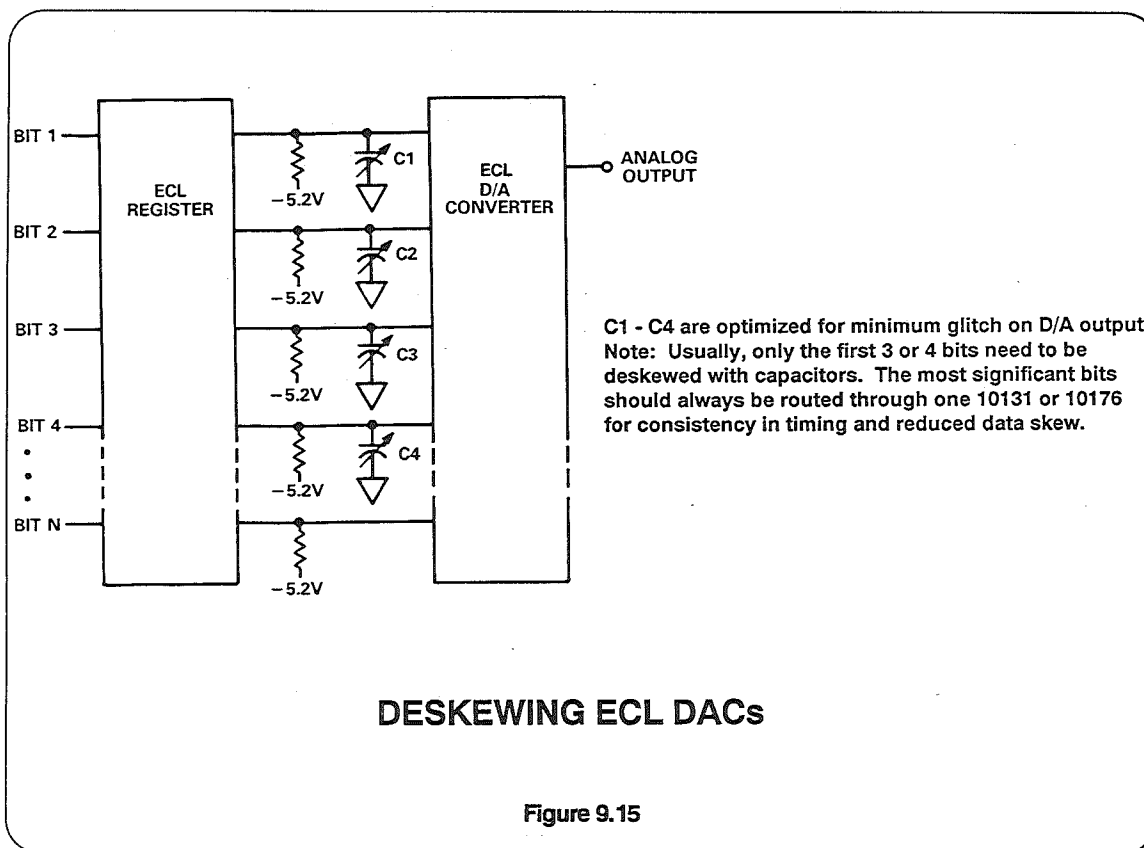
¹ Measurements made on a modified version of the circuit shown in Figure 13, with a 1V full scale.

² Use care in any scheme that lowers the threshold voltage since the output voltage compliance of the DAC is sensitive to this voltage. If the DAC is to be operated in the voltage output mode, it is strongly suggested that the threshold voltage be set at least 200mV above the output voltage full scale.

For threshold voltage less than +1.4V, drive pin 3 directly with a voltage source and tie pin 14 to ground.

EFFECTS OF THRESHOLD VOLTAGE ON AD-568 GLITCH

Figure 9.14



GLITCH REDUCTION USING SEGMENTATION

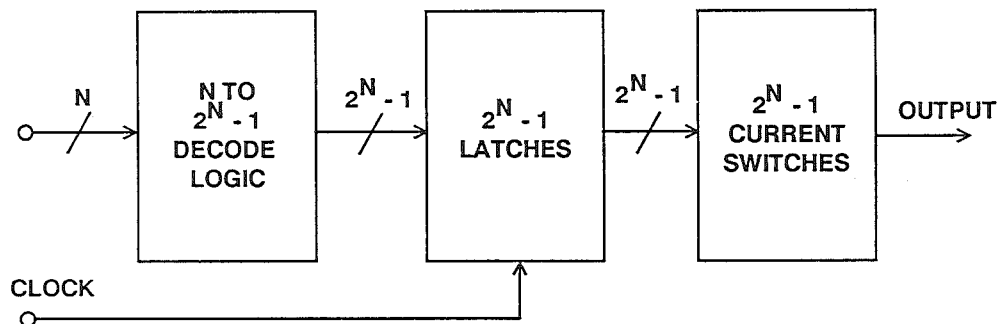
If real estate, cost, power and capacitance were of no consideration, the ideal "glitchless" DAC would consist of $2^N - 1$ equally weighted current switches preceded by decoding logic as shown in Figure 9.16. The glitch produced by switching between levels is code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves.

The scheme shown in Figure 9.16 is not practical for high resolution 12-bit reconstruction DACs, but a significant amount of glitch impulse reduction can be

achieved by applying the concept to the first few MSBs. A block diagram of the AD9712/13 12-bit reconstruction DAC is shown in Figure 9.17 to illustrate the segmented architecture. The four MSBs are decoded into a "thermometer" code which drives 15 equally weighted current switches after latching. The remaining bits are obtained using binary current weighting (bits 5 and 6) and R-2R current division (bits 7-12). Segmentation of the four MSBs reduces the effects of the midscale glitch impulse by a factor of 16 compared to the glitch which would result if straight binary decoding were employed. This technique used in the AD9712 should result in a midscale glitch impulse area of less than 50pV-sec.

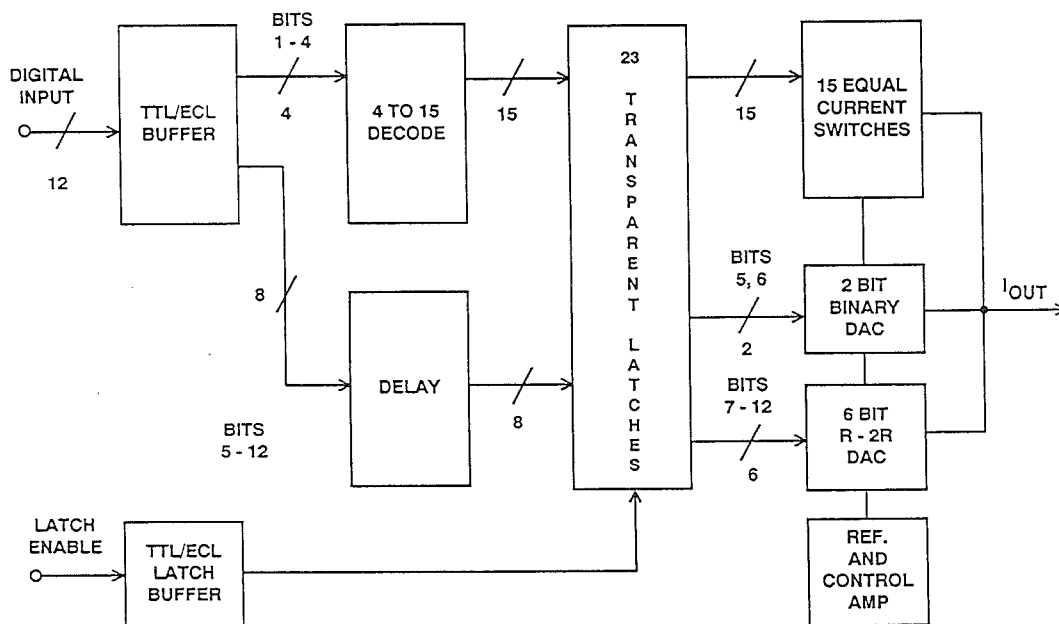
Typical harmonic distortion performance at various update rates for the AD-9712 is

given in Figure 9.18.



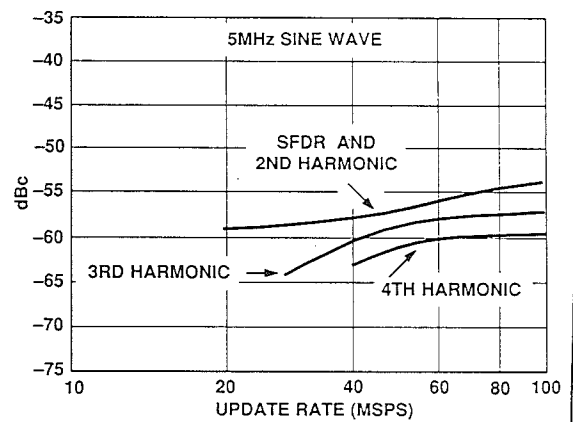
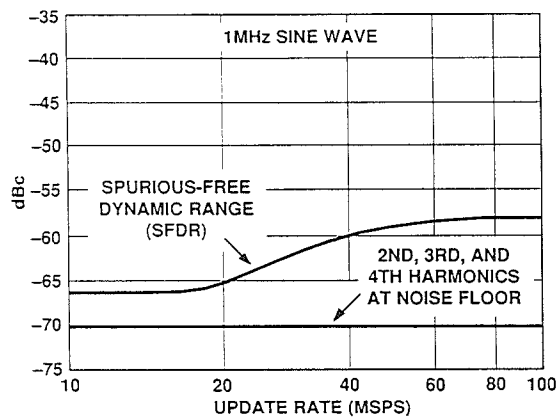
IDEAL DAC FOR MINIMUM GLITCH

Figure 9.16



AD-9712/9713 BLOCK DIAGRAM

Figure 9.17



AD9712 HARMONIC DISTORTION

Figure 9.18

DEGLITCHING USING SHAS

SHAs can be used to deglitch DACs as shown in Figure 9.19. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the

output. The switching transients produced by the SHA are code-independent and occur at the update frequency, hence, they are easily filterable.

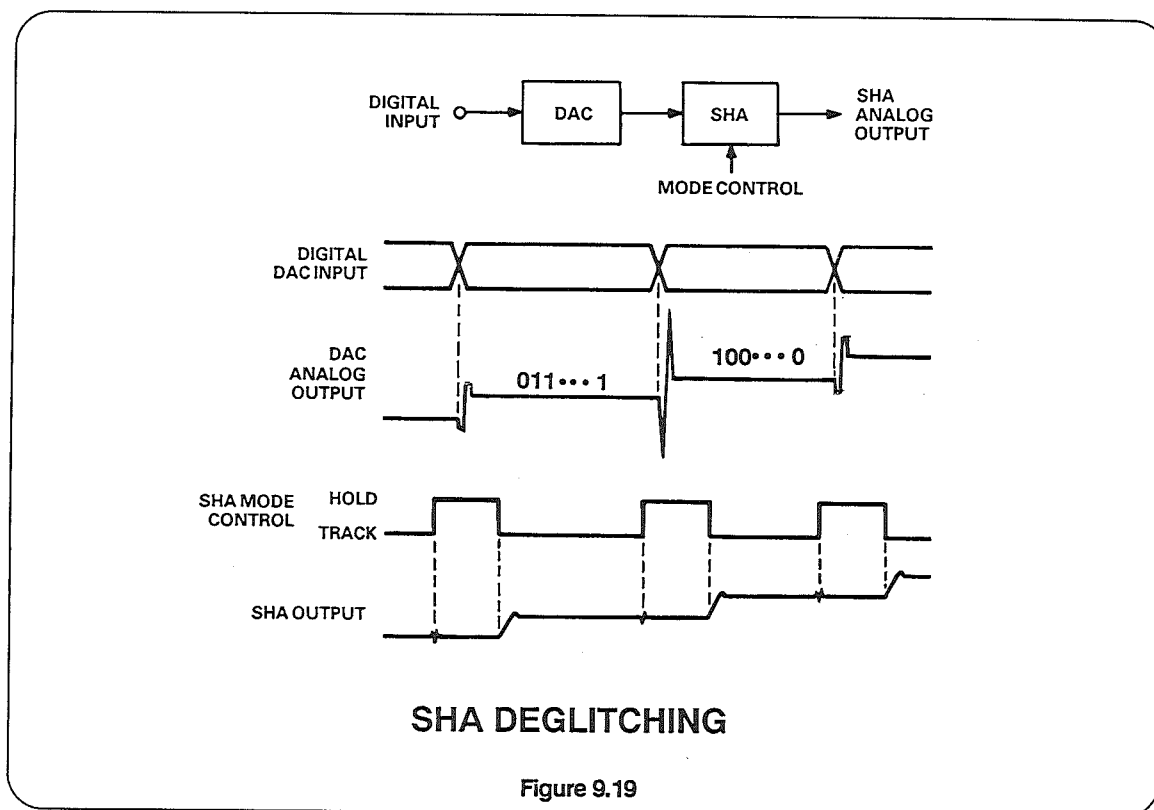
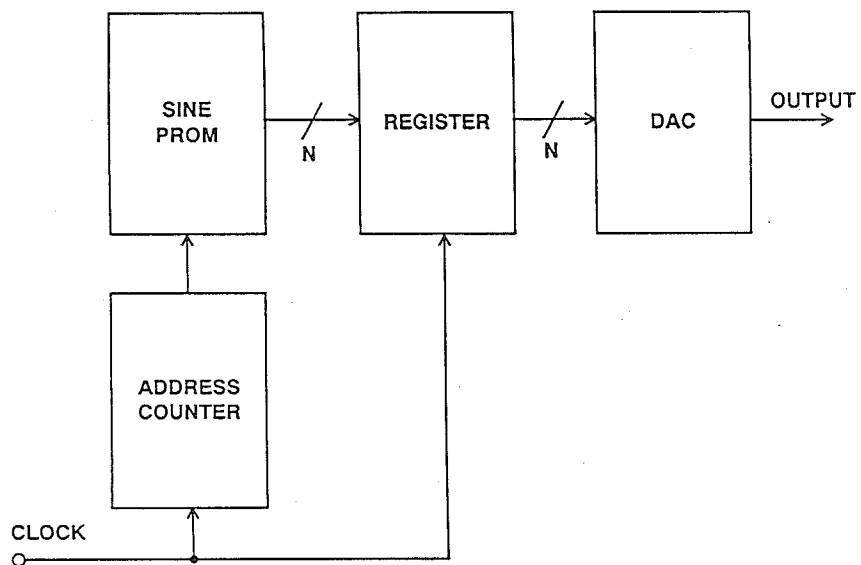


Figure 9.19

DIRECT DIGITAL SYNTHESIS TECHNIQUES

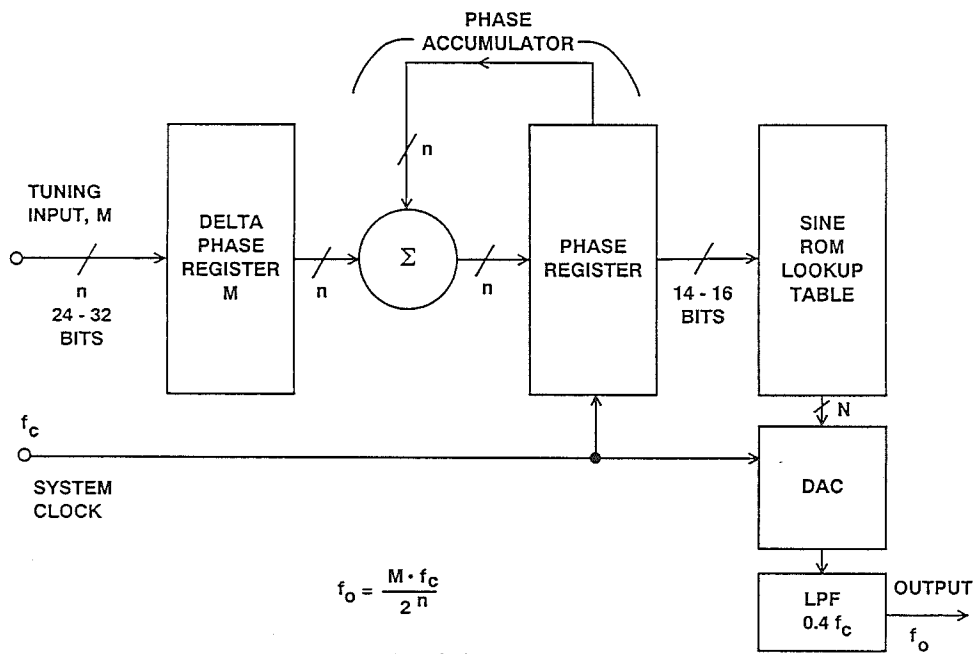
A simple circuit for generating a sine wave using a PROM and a DAC is shown in Figure 9.20. Each location in the PROM corresponds to a discrete sample of the sine wave. Note that the PROM must contain an integer number of cycles in order to prevent a discontinuity from occurring when the PROM "rolls over". In addition, the PROM should contain a prime integer number of cycles of the

sine wave so that the quantization noise is not concentrated in the harmonics of the fundamental. This process is analogous to selecting the proper input sine wave frequency when performing coherent DSP testing on an A/D converter. The simple approach described above is severely limited because the sine wave frequency can only be changed by varying the clock rate or by reprogramming the PROM.



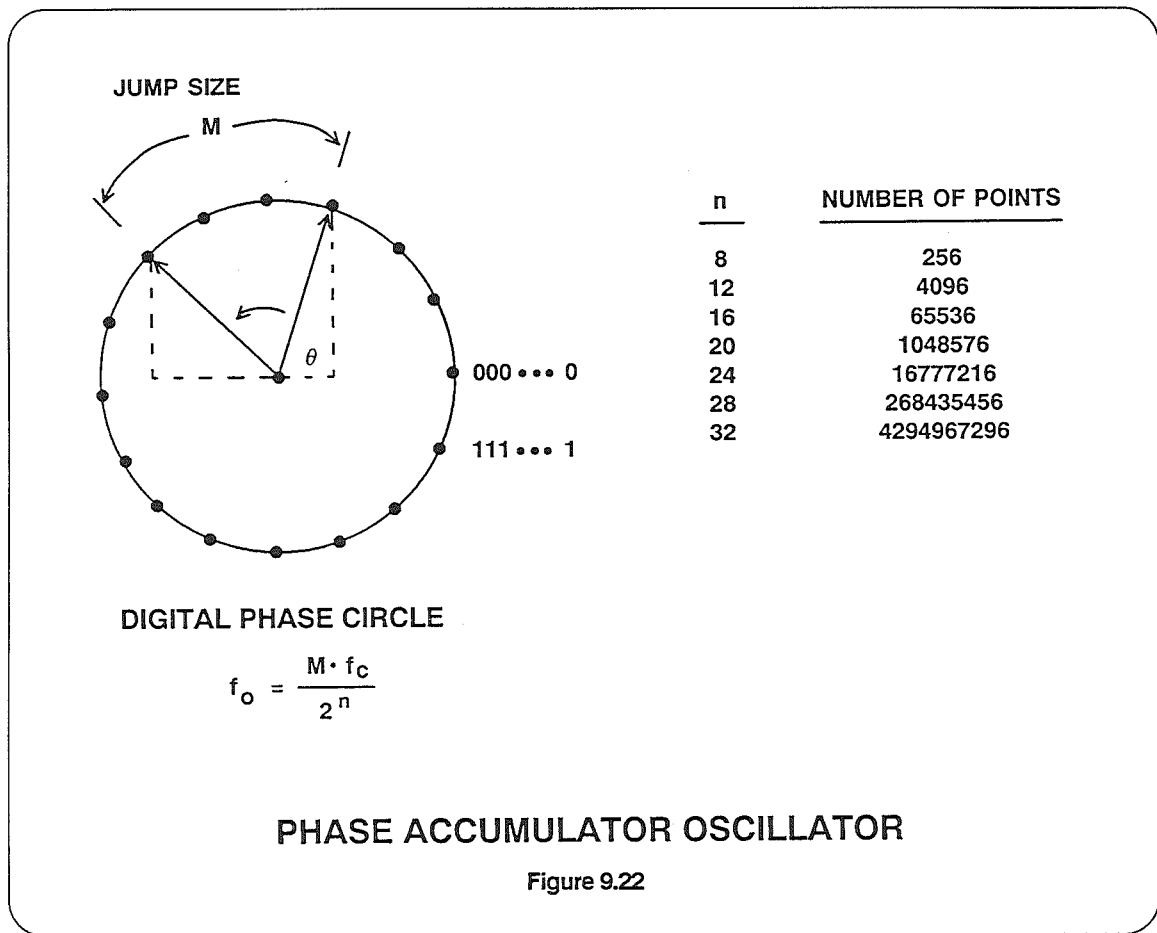
SIMPLE DDS SYSTEM

Figure 9.20



DDS SYSTEM

Figure 9.21



A much more flexible scheme is shown in Figure 9.21 and is the basis of modern DDS techniques. In order to understand how it works, first consider a sinewave oscillation as a vector rotating around a phase circle as shown in Figure 9.22. Each point on the phase circle corresponds to a particular point on the output waveform. As the vector travels around the phase circle, the corresponding output waveform is generated. One revolution on the phase circle corresponds to one complete cycle of the sinewave. A phase accumulator is used to perform the linear motion around the phase circle. The number of discrete points on the phase circle is determined by the resolution of the phase accumulator. For an n-bit accumulator, there are

2^n number of points on the phase circle. The digital word in the delta phase register (M) represents the "jump size" between updates. It commands the phase accumulator to jump by M number of points on the phase circle each time the system is clocked. If M is the number stored in the delta phase register, f_c is the clock frequency, and n is the phase accumulator resolution, then the frequency of rotation around the phase circle (the output frequency) is given by

$$f_o = \frac{M \cdot f_c}{2^n}$$

which is known as the DDS "tuning equation".

Phase Truncation

Note that the frequency resolution of the system is $f_c/2^n$ which represents the smallest incremental frequency capable of being produced. The delta-phase register and the accumulator are typically 24 to 32 bits wide.

The output of the phase accumulator drives the address input of a sinewave ROM lookup table in which is stored amplitude information for exactly one cycle of a sinewave. The ROM thus acts as a phase-to-sine amplitude converter. The output of the ROM drives a DAC which then reconstructs the analog sinewave. Ideally, there is a specific value in the ROM lookup table for each possible phase angle in the accumulator. This can easily result in the need for extremely large ROMs. In practice, the phase data is

usually truncated to reduce the ROM size. The amount of phase resolution directly affects the spectral purity of the output sinewave. If the phase information is truncated to 16-bits, the largest phase spur is about 96dB below the fundamental reconstructed sinewave frequency.

In practice, the phase information is typically truncated to 14-16 bits. A DDS system having 32-bits in the delta-phase register and the accumulator and 16-bits of phase information driving the sine ROM is capable of taxing the state of the art in 12-bit DACs at system clock rates of 30 MHz. Using a low glitch 12-bit DAC such as the AD9712/13 will allow the spurs due to phase truncation and glitch impulse to be kept below -70dBc at a system clock rate up to 30 MHz.

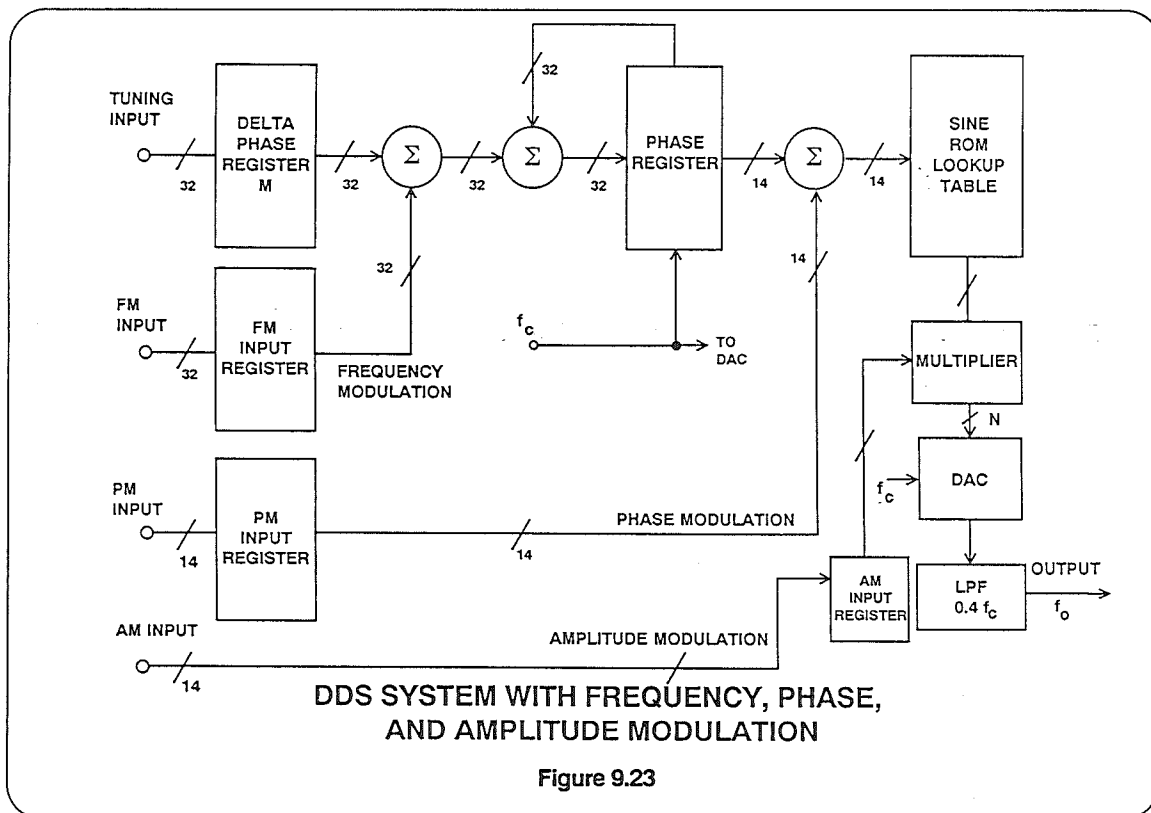


Figure 9.23

A DDS system is capable of generating frequencies ranging from $f_c/2^n$ to $f_c/2$. However, the steepness of the rolloff of the lowpass filter determines the practical upper limit of the output frequency to about 40% of the system clock rate.

If the output frequency is not relatively prime to the system clock frequency, spurious quantization noise will be concentrated in the harmonics of the output frequency. The use of a prime number in the delta-phase register will avoid this effect.

Figure 9.23 shows a DDS system which is capable of frequency, phase, and amplitude modulation. Frequency modulation is achieved by inserting an adder between

the delta phase register and the phase accumulator. The frequency modulator has the same resolution as the phase accumulator thereby enabling frequency modulation over the entire tuning bandwidth. Phase modulation is achieved by inserting an adder after the phase accumulator. Amplitude modulation is achieved by inserting a digital multiplier after the sine ROM lookup table.

A summary of frequency synthesis figures of merit is given in Figure 9.24 and applications for DDS systems are given in Figure 9.25.

A block diagram of a new 300 MHz DDS chip, the AD9950, is shown in Figure 9.26.

FREQUENCY SYNTHESIS FIGURES OF MERIT

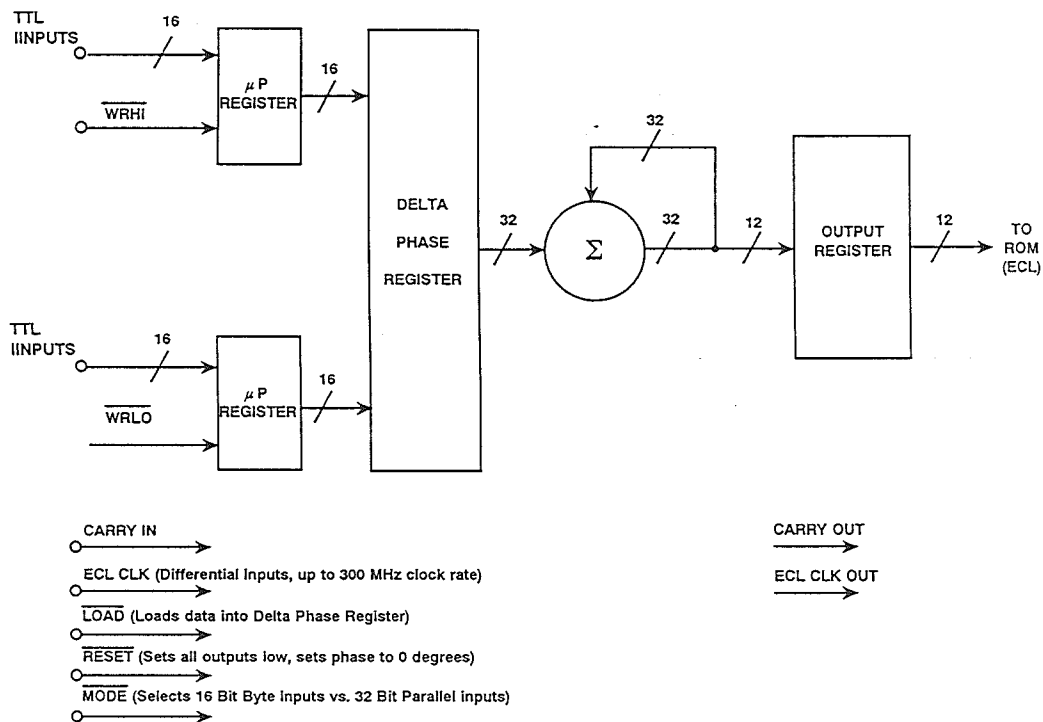
- Tuning Speed
- Resolution (Frequency Step Size)
- Tuning Bandwidth
- Spurious Signal Suppression
- Harmonic Suppression
- Phase Noise

Figure 9.24

DDS APPLICATIONS

- Radio Receiver Local Oscillators
- Signal Generators, Instrumentation
- Frequency Hopping Radios
- Communication Systems
- QAM Systems
- Radar Systems

Figure 9.25



AD9950 BLOCK DIAGRAM

Figure 9.26

HIGH SPEED RECONSTRUCTION DAC SELECTION GUIDE

MODEL	RESOLUTION	SETTLING TIME	COMMENTS
AD9768	8 BITS	5ns	ECL, 20mA Output Current, Int. Ref.
AD565A	12 BITS	250ns	TTL, 5mA Output Current, Int. Ref.
AD568	12 BITS	35ns	TTL, 10mA Output Current, Int. Ref..
AD9712/9713	12 BITS	30ns	ECL/TTL Low Glitch Reconstruction DAC - 100MHz Input Latch

Figure 9.27

